UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,559	08/20/2003	Christopher J. Bostak	200208754-1	6614

22879 7590 01/21/2005

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
CHANG, JOSEPH	
ART UNIT	**PAPER NUMBER**
2817	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,559	BOSTAK ET AL.	
	Examiner	Art Unit	
	Joseph Chang	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,8,11,12 and 14-18* is/are rejected.

7)☒ Claim(s) *2,3,7,9,10,13 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method and system for calibration of a voltage controlled oscillator using a serial resistance ladder for known voltages.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-6, 8, 11, 12, 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Stitt et al. US Pat. No. 5,229,700.

Regarding Claim 1, Stitt et al. discloses a method for calibrating a voltage controlled oscillator (10 of the figure) comprising: applying a plurality of known voltages (VA,VB,VF,VL,VR) to the input of a VCO (20, 40); monitoring (by CPU 18), for each of the voltages, an output count (26, 42) from the VCO (20, 40) over a set interval (intrinsic property of measuring frequency using a counter, see Col. 1, lines 45-51); and storing the output counts for each voltage (counter 26, 42).

Regarding Claim 4. Stitt et al. discloses the method comprising: interleaving a VCO calibration cycle in which known input voltages are substituted for measurements of unknown input voltages.

Regarding Claim 5. Stitt et al. discloses the method comprising: repeating calibration operations for the same known input voltage (VR) at periodic intervals to compensate for variations in operating conditions (Col. 2, lines 56-59).

Regarding Claim 6. Stitt et al. discloses the method comprising: applying an unknown voltage to the VCO input; monitoring an unknown output count from the VCO over a set interval; and comparing the unknown output count to a table of stored output counts (Col. 3, line 44 - Col.4, line14).

Regarding Claim 8. Stitt et al. discloses a system (10 of the figure) for calibrating a voltage controlled oscillator (20,40) comprising: a plurality of known voltages (VA,VB,VF,VL,VR), wherein the known voltage are connectable to the VCO (terminals, see the figure); and a controller (CPU 18) coupled to the output of the VCO (via BUS 30), wherein the controller (18) maintains a calibration table of VCO output counts (26, 42, Col. 4, lines 8-14) for selected voltage inputs (VA,VB,VF,VL,VR).

Regarding Claim 11, Stitt et al. discloses that a plurality of VCOs (20,40); and wherein the controller (18) maintains a separate calibration table for each of the VCOs (Col.4, lines 8-14).

Regarding Claim 12. Stitt et al. discloses a computer program product comprising a computer usable medium (Col.3, lines 5-10) having computer readable program code embedded therein (inherent property of CPU 18), the computer readable program code comprising: code for selecting a voltage to be applied to inputs of a plurality of voltage controlled oscillators; code for monitoring output counts from each of the plurality of VCOs over a set period of time, while the selected voltage is applied to

the VCOs' inputs; and code for storing, for each of the plurality of VCOs, a table of output counts associated with the selected voltage (the same as the scope of Claim 1 with inherency of CPU 18).

Regarding Claim 14, Stitt et al. discloses a computer program product of code for interleaving a VCO calibration cycle during which with other VCO measurements (Col. 1, lines 25-36)

Regarding Claim 15, Stitt et al. discloses a system (10) for calibrating a voltage controlled oscillator (20, 40) comprising: means for applying a plurality of known voltages (VA,VB,VF,VL,VR through resisters 22a-f, 24a-f) to the input of a VCO (20, 40); means for monitoring (CPU 18), for each of the voltages(VA,VB,VF,VL,VR), an output count from the VCO (20, 40) over a set interval; and means for storing (26, 42) the output counts for each voltage.

Regarding Claim 16, Stitt et al. discloses the system comprising: means for interleaving a VCO calibration cycle in which known input voltages (VA,VB,VF,VL,VR) are substituted for measurements of unknown input voltages (Col. 1, lines 25-36).

Regarding Claim 17. Stitt et al. discloses the system comprising: means for repeating calibration operations for the same known input voltage at periodic intervals to compensate for variations in operating conditions (Col. 1, lines 25-36).

Regarding Claim 18, Stitt et al. discloses the system comprising: means for applying an unknown voltage (VA,VB,VF,VL,VR) to the VCO input (via resisters 22a-f and 24a-f. 34,36,38); means for monitoring (CPU 18) an unknown output count from the VCO over a set interval (intrinsic property of measuring frequency using a counter, see

Col. 1, lines 45-51); and means for comparing the unknown output count to a table of stored output counts (Col.4, lines 8-14).

Allowable Subject Matter

Claims 2,3,7,9,10,13,19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the best prior art of record, Stitt et al, taken alone or in combination of other references, does not teach or fairly suggest a serial resistance having a plurality of equal resistors (or voltage taps).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Newell discloses a control circuit having a VCO, a counter and a DAC.

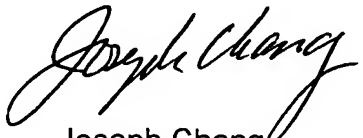
Zuta discloses a frequency synthesizer including a VCO counter.

Schousek et al. discloses a battery monitoring circuit having a CPU, a VCO, a calibration circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Chang whose telephone number is 571 272-1759. The examiner can normally be reached on Mon-Fri 0700-1730.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph Chang
Patent Examiner
Art Unit 2817